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EXAMINER	
LEE, CHRISTOPHER E	

ART UNIT	PAPER NUMBER
2112	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/937,468	HEIGHWAY ET AL.	
	Examiner	Art Unit	
	Christopher E. Lee	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25 and 27* is/are allowed.

6)☒ Claim(s) *1,4-7,9-12,15-19,21-24 and 26* is/are rejected.

7)☒ Claim(s) *2,3,8,13,14 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Receipt Acknowledgement

1. Receipt is acknowledged of the Amendment filed on 11th of July 2005. Claims 8, 22, 23, 25, and 26 have been amended; no claim has been canceled; and no claim has been newly added since the RCE Non-Final Office Action was mailed on 29th of March 2005. Currently, claims 1-27 are pending in this Application.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by Bunting et al. [WO 95/15651; hereinafter Bunting].

Referring to claim 1, Bunting discloses a method for assembling data packets (See page 1, lines 5-9) for isochronous data transmission (See page 4, lines 7-17; i.e., wherein in fact that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packet unit exhibit proper time synchronism inherently anticipates that said data packets are for isochronous data transmission) via a data bus (i.e., via Transmission Channel in Fig. 19), a data format for said isochronous data transmission being defined in an isochronous data format header of said data packet (See page 5, line 29 through page 6, line 2; i.e., wherein in fact that each header contains information related to the data in the data packet with which the header is associated, and the header information aids data assembly and synchronization at a receiver, and includes information such as service type, frame type, frame number and slice number inherently anticipates that a data format for said isochronous data transmission is defined in an isochronous data format header of said data packet), comprising the steps of: writing said

isochronous data format header to a special register (i.e., Output Register 78 of Fig. 17) and to a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17) for said data packets (i.e., in fact, Header is written to said Header FIFO and also written to said Output Register and said Rate Buffers in the form of being combined with Data) when said isochronous data transmission is set up in a data transmitting device (i.e., setting up in a video signal encoder; See page 2, lines 27-30, and page 3, lines 30+); and attaching (i.e., combining) useful data of said data packet (i.e., packed data words) to said isochronous data format header (i.e., Header) in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Output Register and said Rate Buffers; See page 5, lines 11-28); and taking both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

Referring to claim 4, Bunting teaches selecting same number of data blocks per data packet (See page 3, lines 30-34; i.e., wherein in fact that 960 bits per data packets anticipates selecting same number of data blocks per data packet).

Referring to claim 6, Bunting discloses an apparatus (i.e., video signal encoder in Fig. 1) for carrying out said method according to claim 1 (See claim 1 rejection), comprising a buffer memory for data packets (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17), having a special register (i.e., Output Register 78 of Fig. 17) for said isochronous data format header (i.e., Header) of one of said data packets (i.e., Output Register 78 including said Header in the form of being combined with Data in Fig. 17), and having initialization means (i.e., FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17), which copy said isochronous data format header for a first data packet of said isochronous data transmission to said special register for said isochronous data format header and said buffer memory (See page 14, lines 19+; i.e., copying Header for data packet word of isochronous data transmission to Output Register for combining

said Header, and being stored in said Rate Buffers 713 and 714 in Fig. 19), and transmission means (i.e., Modem 717 of Fig. 19) for reading (i.e., retrieving and transmitting) both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

Referring to claim 7, Bunting teaches said isochronous data format header (i.e., Header) for said first data packet is prescribed for said initialization means (i.e., said Header is generated by Header Generator 18 of Fig 1 for said FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17) by an application process (i.e., by digital television signal processing; See Abstract).

Referring to claim 9, Bunting discloses a method for assembling data packets for data transmission (See page 1, lines 5-9) via a data bus (i.e., via Transmission Channel in Fig. 19), said method comprising: writing a data header (i.e., Header) to a special register (i.e., Output Register 78 of Fig. 17) and to a selected portion (i.e., Header FIFO 70 of Fig. 17) of a buffer memory for said data packets (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17); and appending (i.e., combining) useful data in a form of data blocks (i.e., packed data words) to said data header (i.e., Header) located in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Rate Buffers; See page 5, lines 11-28); and taking both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

Referring to claim 15, Bunting teaches selecting a same number of data blocks per data packet (See page 3, lines 30-34; i.e., wherein in fact that 960 bits per data packets anticipates selecting same number of data blocks per data packet).

Referring to claim 18, Bunting discloses an apparatus (i.e., video signal encoder in Fig. 1) for assembling data packets for data transmission (See page 1, lines 5-9) via a data bus (i.e., via Transmission Channel in Fig. 19), comprising: a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17) for said assembly of data packets

(i.e., combining Header and Data; See page 14, lines 27-33); a special register (i.e., Output Register 78 of Fig. 17) for storing a data header (i.e., Header) of a first one of said data packets (i.e., Output Register 78 including said Header in the form of being combined with Data in Fig. 17); and an initialization means (i.e., FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17) for copying said data header for said first data packet to said special register and to said buffer memory (See page 14, lines 19+; i.e., copying Header for data packet word of isochronous data transmission to Output Register for combining said Header, and being stored in said Rate Buffers 713 and 714 in Fig. 19); and transmission means (i.e., Modem 717 of Fig. 19) for reading (i.e., retrieving and transmitting) both said isochronous data format header and said useful data from said buffer memory for data transmission (See page 19, lines 3-15).

Referring to claim 19, Bunting teaches said data header (i.e., Header) for said first data packet is prescribed by an application process (i.e., said Header is generated by Header Generator 18 of Fig 1 for said FIFO State Controller 74 and Header/Data Multiplexer 76 in Fig. 17 of digital television signal processing; See Abstract).

Referring to claims 10, 11, 21 and 22, Bunting teaches said data packets are isochronous data packets, and said data bus is an isochronous data bus (See page 4, lines 7-17; i.e., wherein in fact that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packet unit exhibit proper time synchronism inherently anticipates that said data packets are isochronous data packets, and said data bus is an isochronous data bus).

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 5, 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunting [WO 95/15651] as applied claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 above, and further in view of what was well known in the art, as exemplified by Takayama [US 5,991,842 A].

Referring to claims 5, 16 and 17, Bunting discloses all the limitations of the claims 5, 16 and 17, respectively, except that does not teach dividing said data to be transmitted into data source packets, wherein, in particular for said transmission of MPEG2 video data; a data source packet is composed from 8 data blocks.

The Examiner takes Official Notice that dividing said data to be transmitted into data source packets, wherein, in particular for said transmission of MPEG2 video data, a data source packet is composed from 8 data blocks, is well known to one of ordinary skill in the art, as evidenced by Takayama (See col. 9, lines 33-44).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to have applied said method step of dividing said data source packets into 8 data blocks, as disclosed by Takayama, to said method, as disclosed by Bunting, since it would have ensured a communications being performed by using said data bus (i.e. 1394 serial bus) at a predetermined communication cycle (See Takayama, Fig. 6 and col. 5, lines 24-31).

6. Claims 12 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunting [WO 95/15651] as applied claims 1, 4, 6, 7, 9-11, 15, 18, 19, 21 and 22 above, and further in view of Sato et al. [US 6,259,694 B1; hereinafter Sato].

Referring to claims 12 and 23, Bunting discloses all the limitations of the claims 12 and 23, respectively, except that does not teach said data header comprising a comparison value for counting data blocks.

Sato discloses a method of enabling an error bit to be set simply without causing an increase in the size of signal processing circuit (See Abstract), wherein a data header (i.e., CIP Header in Fig. 14) comprising a

comparison value (i.e., data block continuity counting value in DBC field of Fig. 14) for counting data blocks (i.e., detecting the number of the isochronous packets; See col. 10, lines 54-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said comparison value for counting data blocks (i.e., DBC field), as disclosed by Sato, in said data header, as disclosed by Bunting, for the advantage of indicating discontinuity when it detects the discontinuity of the DBC (i.e., indicating packet loss; See Sato, col. 10, line 66 through col. 11, line 6).

7. Claims 24 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunting [WO 95/15651] in view of Sato [US 6,259,694 B1].

Referring to claim 24, Bunting discloses a method for assembling data packets (See page 1, lines 5-9) for isochronous data transmission (See page 4, lines 7-17; i.e., wherein in fact that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packet unit exhibit proper time synchronism inherently anticipates that said data packets are for isochronous data transmission) via a data bus (i.e., via Transmission Channel in Fig. 19), a data format for said isochronous data transmission being defined in an isochronous data format header of a bus packet (See page 5, line 29 through page 6, line 2; i.e., wherein in fact that each header contains information related to the data in the data packet with which the header is associated, and the header information aids data assembly and synchronization at a receiver, and includes information such as service type, frame type, frame number and slice number inherently anticipates that a data format for said isochronous data transmission is defined in an isochronous data format header of a bus packet), comprising the steps of: writing said isochronous data format header to a special register (i.e., Output Register 78 of Fig. 17) and to a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713

and 714, shown in Fig. 17) for said data packets (i.e., in fact, Header is written to said Header FIFO and also written to said Output Register and said Rate Buffers in the form of being combined with Data) when said isochronous data transmission is set up in a data transmitting device (i.e., setting up in a video signal encoder; See page 2, lines 27-30, and page 3, lines 30+); and attaching (i.e., combining) useful data of said data packet (i.e., packed data words) to said isochronous data format header (i.e., Header) in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Output Register and said Rate Buffers; See page 5, lines 11-28).

Bunting does not teach said isochronous data format header including a comparison value generated by a data block counter for data block counting.

Sato discloses a method of enabling an error bit to be set simply without causing an increase in the size of signal processing circuit (See Abstract), wherein an isochronous data format header (i.e., CIP Header in Fig. 14) including a comparison value (i.e., data block continuity counting value in DBC field of Fig. 14) generated by a data block counter (i.e., counter for detecting the number of the isochronous packets) for data block counting (i.e., detecting the number of the isochronous packets; See col. 10, lines 54-55). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said comparison value for data block counting (i.e., DBC field), as disclosed by Sato, in said data header, as disclosed by Bunting, for the advantage of indicating discontinuity when it detects the discontinuity of the DBC (i.e., indicating packet loss; See Sato, col. 10, line 66 through col. 11, line 6).

Referring to claim 26, Bunting discloses a method for assembling data packets for data transmission (See page 1, lines 5-9) via a data bus (i.e., via Transmission Channel in Fig. 19), said method comprising: writing a data header (i.e., Header) to a special register (i.e., Output Register 78 of Fig. 17) and to a selected portion (i.e., Header FIFO 70 of Fig. 17) of a buffer memory for said data packets (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713

and 714, shown in Fig. 17); and appending (i.e., combining) useful data in a form of data blocks (i.e., packed data words) to said data header (i.e., Header) located in said buffer memory (i.e., combining Data from said Data FIFO with Header in said Header FIFO are stored in said Rate Buffers; See page 5, lines 11-28).

Bunting does not teach said data header comprising a comparison value for counting data blocks, said comparison value is a number of data blocks, and said comparison value relates to a first data block in said data packet.

Sato discloses a method of enabling an error bit to be set simply without causing an increase in the size of signal processing circuit (See Abstract), wherein a data header (i.e., CIP Header in Fig. 14) comprising a comparison value (i.e., data block continuity counting value in DBC field of Fig. 14) for counting data blocks (i.e., detecting the number of the isochronous packets; See col. 10, lines 54-55), said comparison value is a number of data blocks (See col. 10, line 55; actually, the number of the isochronous packets in DBC region shows a number of data blocks), and said comparison value relates to a first data block in said data packet (in fact, the number of data blocks in DBC region are in sequence from the first source packet for indicating a potential discontinuity error; See col. 10, line 66 through col. 11, line 6).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said comparison value for counting data blocks (i.e., DBC field), as disclosed by Sato, in said data header, as disclosed by Bunting, for the advantage of indicating discontinuity when it detects the discontinuity of the DBC (i.e., indicating packet loss; See Sato, col. 10, line 66 through col. 11, line 6).

Allowable Subject Matter

8. Claims 25 and 27 are allowed.

9. Claim 2, 3, 8, 13, 14 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. The following is a statement of reasons for the indication of allowable subject matter:

The limitations of claims 2, 8, 13 and 20 are respectively deemed allowable over the prior art of record as the prior art fails to teach or suggest that updating (transferring) said comparison value in said data header in said special register when said useful data in data blocks are written to said buffer memory, and copying said updated data header to said buffer memory at a next free location for a data packet in said buffer memory. The claim 3 is a dependent claim of the claim 2, and the claim 14 is a dependent claim of the claim 13.

The limitations of claim 25 is deemed allowable over the prior art of record as the prior art fails to teach or suggest that a memory management unit transfers a counter reading of the data block counter after the counting of the data blocks of said one of said data packets to the isochronous data format header stored in the special register, and copies the isochronous data format header that has been updated in this way in the special register to the buffer memory at the beginning of the next free location for said one of said data packets.

The limitations of claim 27 is deemed allowable over the prior art of record as the prior art fails to teach or suggest that a data block counter transfers a count in said data block counter to said data header stored in said special register, and further wherein said count in said special register is copied to said buffer memory at a next free location.

Response to Arguments

11. Applicants' arguments filed on 11th of July 2005 have been fully considered but they are not persuasive, and the Examiner notes that the Office Action mailed on 29th of March 2005 was not the Final Office Action, but the Non-Final Office Action, in regard to the remarks in lines 2-3 on page 8.

In response to the Applicants' response with respect to "... It should further be noted that since an inventor can be his own lexicographer, the inventors have defined "isochronous" with respect to the present application at page 1, line 37 to page 2, line 1, as "that data to be transmitted arise regularly at a data source, the data also arising with approximately the same size each time." In particular, the present application nowhere discusses the use of a clock signal or any delay. ... The Examiner has indicated that is "anticipates that said data packets are the isochronous data transmission". Applicants fail to recognize that the above description in Bunting anticipate isochronous data transmission as defined by the inventors for the present invention given that the present invention does not use a clock signal or any form of delay. Further, Bunting requires a PAF "to ascertain the completion of 32-bit data words, assembled from a stream of variable length codewords, and the completion of 960-bit long data packets." ..." on the Response page 8, line 27 through page 10, line 2, the Examiner respectfully disagrees.

Basically, Bunting describes that input processor unit includes a signal delay network for processing the picture start code-word and the PAP so that the PAF occurs in the code word clock cycle immediately before the I frame picture start codeword, and the delay network assures that the output signals applied to packed word controller unit and data packet unit exhibit proper time synchronism on page 4, lines 7-17, which inherently anticipates that the data packets are for isochronous[1] data transmission (i.e., with exhibiting proper time synchronism) via a data bus (i.e., via Transmission Channel).

In contrary to the Applicants' assertion, Bunting suggests isochronous data transmission, such that packed data and header (i.e., data) to be transmitted arise regularly at a data source (i.e., the output signals applied to packed word controller unit and data packet unit exhibit proper time synchronism), the packed data and header (i.e., data) also arising with approximately the same size each time (See Bunting, page 6, lines 3-21).

[1] In the specification, page 1, line 37 through page 2, line 1, the Applicants define the claimed subject matter "isochronous" means data to be transmitted arise regularly at a data source, the data also arising with approximately the same size each time.

Furthermore, even though the Applicants assert that the claimed invention does not use a clock signal or any form of delay, which are shown in Bunting's invention, it is noted that the features upon which applicants rely (i.e., the claimed invention does not use a clock signal or any form of delay) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the above argued elements are inherently anticipated by Bunting as have been discussed above, and the Applicants' arguments on this point is not persuasive.

In response to the Applicants' argument with respect to "Further, the Examiner points to buffer memory including Header FIFO 70, Data FIFO 72 and Rate buffers 713 and 714. ... Header FIFO 70 and Data FIFO 72 do not read on claim 1 because as recited in claim 1 there is a " taking both the isochronous data format header and the useful data from said buffer memory for data transmission" that does not occur in Bunting. ... The design of Data and Header Combiner 15 shows that during set up of a data transmission the header data is written into the Header FIFO 70 only. That is, there is no bus connection between Header Generator 18 and Output Register 78 or Rate Buffers 713 and 714. ... Therefore, writing of the header to the special register and to the buffer memory during set up of an isochronous data transmission does not occur. Further, the Output Register 78 of Bunting, while denominated "register", is in fact not a register. On page 16, lines 6-9 it is explained that component 78 is an Output Buffer in which storage capacity for more than a complete packet is available. ..." in the Response page 10, lines 3-30, the Examiner respectfully disagrees.

In fact, the Examiner shows that Bunting teaches the claimed subject matters "special register" as Output Register 78 and "buffer memory" as Buffer Memories, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714 in Fig. 17. And thus, the scope of the claimed invention has been taught by Bunting, such that, writing said isochronous data format header to a special register (i.e., Output Register 78 of Fig.

17) and to a buffer memory (i.e., Buffer Memories of Bunting, such that Header FIFO 70, Data FIFO 72, Rate Buffers 713 and 714, shown in Fig. 17) for said data packets (i.e., in fact, Header is written to said Header FIFO and also written to said Output Register and said Rate Buffers in the form of being combined with Data) when said isochronous data transmission is set up in a data transmitting device (i.e., setting up in a video signal encoder; See Bunting, page 2, lines 27-30, and page 3, lines 30+), in particular. Even though said Header FIFO and Data FIFO of Bunting are not separately read in the claim 1, said Buffer Memories of Bunting, i.e., Header FIFO, Data FIFO, Rate Buffers, could be properly interpreted as the claimed subject matter "buffer memory", and thus the argued limitation is taught by Bunting as have been discussed above in contrary to the Applicants' statement.

In addition, the Applicants argues that Bunting's element "Output Register" is not a register, but "Output Buffer." However, Bunting clearly shows Output Register 78 in Fig. 17. Even though Bunting mentions Output Register 78 in Fig. 17 as an Output Buffer in line 6 on page 16, both of the terms "Output Buffer" and "Output Register" are used for performing the function of register in the art[2].

Furthermore, in contrary to the Applicants' argument, i.e., there is no bus connection between Header Generator 18 and Output Register 78 or Rate Buffers 713 and 714, and thus, writing of the header to the special register and to the buffer memory during set up of an isochronous data transmission does not occur, Bunting teaches the argued limitation as have been discussed above paragraph 3 of the instant Office Action, claim 1 rejection under 35 U.S.C. 102(b) as being anticipated by Bunting regardless of a bus connection between header generator and output buffer.

Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Independent claims 6, 9 and 18 have features similar to those recited in claim 1. Specifically, while claims 9 and 18 do not recite isochronous data transmission, they do recite the use of a register and a buffer memory, which are distinguishable over

[2] "register" being defined as "a device capable of retaining information, often that contained in a small subset, of the aggregate information in a digital computer" *IEEE Standard Dictionary of Electrical and Electronics Terms, 3rd edition.*

those described in Bunting as explained above. It is, therefore submitted that claims 6, 9 and 18 are also not anticipated and patentable over the art of record." in the Response page 11, lines 1-5, and "Independent claim 26 does not recite isochronous data transmission, but does recite the use of a register and a buffer memory, which are distinguishable over those described in Bunting as explained above. It is, therefore, respectfully submitted that independent claim 24 and 26 are also unanticipated and patentable over the art of record." in the Response page 12, lines 2-6, the Examiner respectfully disagrees.
In fact, the claimed subject matter "the use of a register and a buffer memory" is clearly anticipated by Bunting as have been discussed above.
Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Regarding claims 5, 16 and 17, Takiyama describes the format of a CIP packet and that a source packet may be divided in a number of data blocks, but is silent to how the CIP packet is formed in memory. In particular, Takiyama does not describe the use of a single buffer (or FIFO) for assembling data or simplification of the method and circuitry required for assembling data packets by omitting a selection logic unit from the combiner circuitry." in the Response page 11, lines 6-11, the Examiner believes that the Applicants misinterpret the claim rejection. The Applicants essentially argue that Takayama doesn't teach the above argued elements. However, Bunting teaches the above argued elements, and therefore, the combination of Bunting and Takayama with rationale suggests the obviousness of the claimed invention.
Thus, the Applicants' argument on this point is not persuasive.

In response to the Applicants' argument with respect to "Regarding claims 12 and 23, Sato describes in detail the isochronous cycle of a IEEE 1394 bus inclusive of the isochronous bus packet format and the late check (error bit). Sato also describes ... Data flow in Fig. 5 is from FIFO 110 to Link Core 101 via post processing unit 107. The CIP header is added to the source packet 'On the Fly'. This

teaches away from the present invention in which both the CIP header and the source packet data is taken/read from the buffer memory. ... " in the Response page 11, lines 12-19, the Examiner believes that the Applicants misinterpret the claim rejection.

The Applicants essentially argue that Sato teaches away from the present invention in which both the CIP header and the source packet data is taken/read from the buffer memory. However, Bunting teaches the above argued elements, and therefore, the combination of Bunting and Sato with rationale suggests the obviousness of the claimed invention.

Thus, the Applicants' argument on this point is not persuasive.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher E. Lee whose telephone number is 571-272-3637. The examiner can normally be reached on 9:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christopher E. Lee
Examiner
Art Unit 2112

CEL/ CEL

REHANA PERVEEN
PRIMARY EXAMINER
10/1/05